Pass Through Circuit for Reduced Memory Latency in a Multiprocessor System

ABSTRACT

A technique and mechanism for reducing memory latency asymmetry in a multiprocessor system by replacing one (or more) processors with a bypass or pass-through device. Using the pass-through mechanism, the reduced number of processors in the system enables all of the remaining processors to connect to each other directly using the interconnect links. The reduction in processor count improves symmetry and reduces overall latency thereby potentially improving performance of certain applications despite having fewer processors. In one specific implementation, the pass through device is used to connect two HyperTransport links together where each of the links is connected to a processor at the other end.